

1/2

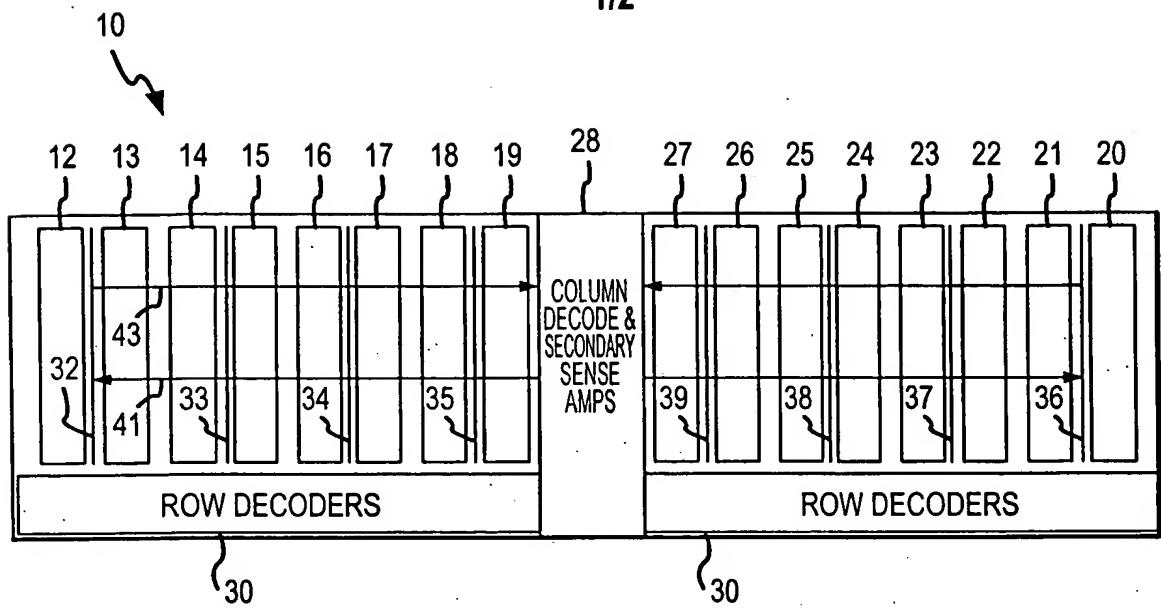


FIG. 1  
(PRIOR ART)

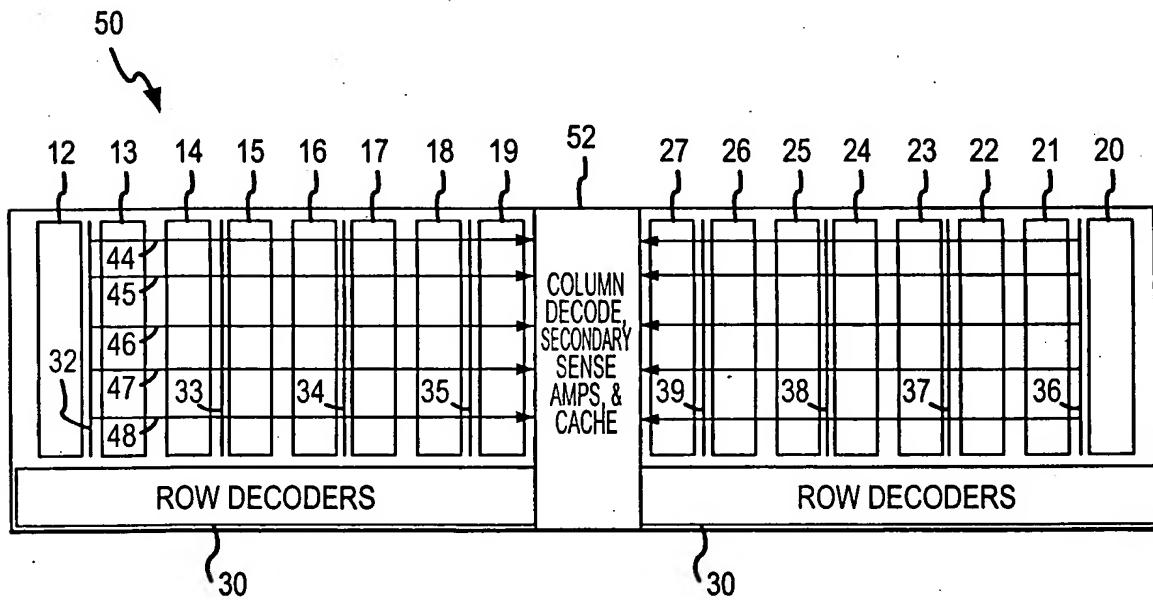


FIG. 2

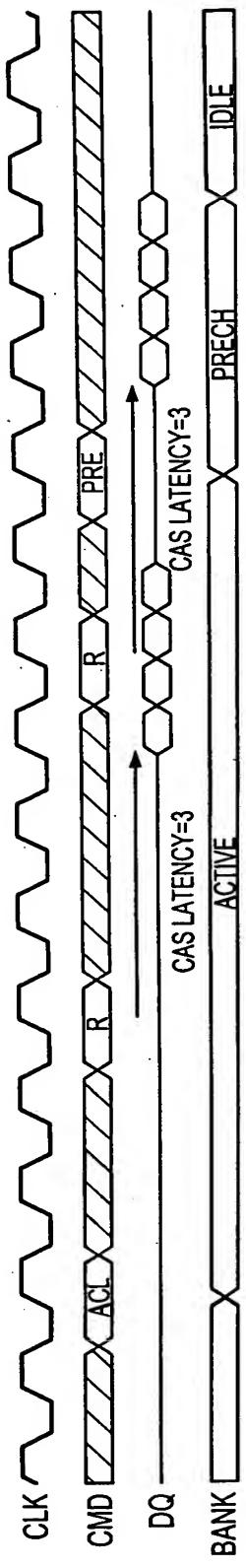
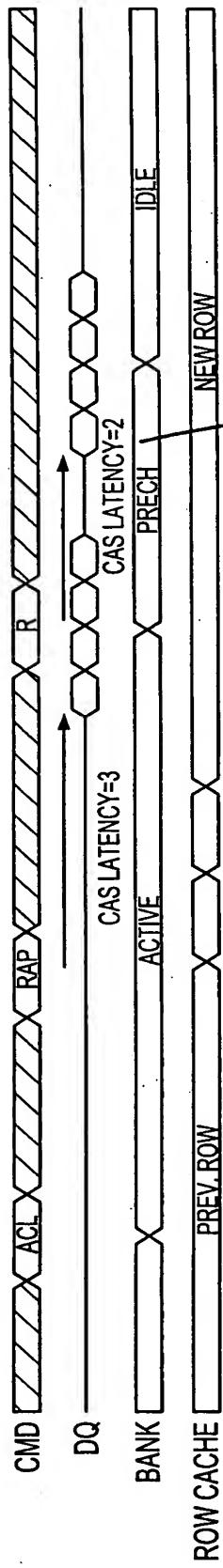


FIG.3



ROW CACHE COMPLETELY LOADED BY THIS POINT

SUBSEQUENT ACCESS TO ROW CACHE OCCURS WITH LOWER LATENCY (CL2)

